Prithivish Shivdasani

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**Senior Technical lead/Engineer**

Qualified senior software professional with 15+ years of experience in catering to projects across diverse organizations including product software development (device drivers and system software/firmware) & 7+ years in system validation using C and scripts. Hold extensive experience in working on emulated platforms like FPGA, and simulators like palladium. Have created Linux BSPs for a variety of chips/boards. Expertise in SAS/SATA/AHCI, familiarity with PCIe. General expertise in any communication protocol validation. Advanced user of tools and technologies like, debuggers, JTAG ICEs, packet sniffers, protocol analyzers, oscilloscopes and logic analyzers. Proficient in programming bare metal. Exploring challenging opportunities requiring senior individual contribution or technical leadership in embedded system and/or general system, IoT/IoE, domains that require software development and/or project / program management.

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| Expertise in   * C Programming * Pre & Post Silicon Validation * SAS/SATA/ AHCI Storage domain protocol * Communication protocol validation * Hardware aware software development. * Systems/kernel Programming. Device driver development. * Project implementation & People management * Manual test and automation. * Troubleshooting & Debugging * OO programming in C++/Python * Boot loader development for ARM targets. * Requirement Analysis * Automation Strategy/ planning/implemention * Client Interaction * Cross Functional Team Coordination * WMI SDK and WfM compliant software development   Education   * **B E (Computer Engineering),** University of Pune | Executive Summary   * Proficient in working on protocol driven communication, validation of storage domain protocols like SAS, SATA, AHCI. Generally skilled in diagnostic software development for communication protocol/hardware validation and test. * Extensive embedded C/C++ application development over RTOS . OO Python development for enhancement of system/platform interfaces. * Skilled in conducting module / partition level validation, pre and post silicon validation, using tools like Protocol analyzer, logic analyzer, Oscilloscopes, Bus doctors etc * Experienced in software development of GPS/location intelligence, telematics, navigation applications for handheld and automotive industrial domains, working on embedded systems / Kernel programming. Working with gyros, accelerometers, MEMS sensor devices/chips, in general. * Hardware aware software/ device drivers, in C /Assembly. Good knowledge of OSes like ThreadX, FreeRTOS, OpenRTOS, Linux / RTLinux and Windows CE. * BSP creation and testing on multiple chips/boards. * Microcontroller programming(Keil). * Familiarity with development platforms like FPGA and Palladium. * Adept at identifying client’s need to be translated into appropriate technical solutions, managing escalations, issues and risks * Network device driver testing. L2 layer testing for switch. Peer to Peer testing. * Test and validation experience in key peripheral interfaces like SPI, I2C, UART etc. * Project planning, people management using scrum/agile methods. * Efficient Team Leader & Player, combining communication, interpersonal & problem solving skills with analytical, decision making and leadership capabilities. Experienced in co ordinating with functionally different teams, managing, hardware software resource and scheduling requirements to make program a success. |

Professional Experience

**Broadcom, Bangalore  Dec 2014 – Mar 2016**

**Principal Engineer PSV**

**Accountabilities:**

* Functioned as team lead / technical lead for multiple projects on dissimilar technologies. Involved in managing team metrics & productivity
* Optimized resource utilization by allocating multiple work items to members across multiple projects for maintaining project delivery schedules
* Developed & implemented automation strategy, defined review criteria for developed C code and scripts. Architected and managed test development
* Focused on design, development & implementation of complex code for silicon validation of designed modules. Collaborated with logic designers in evaluating operation on block & system levels
* Investigated use cases, system-level operation, and performance requirements. Developed low-level software to validate functionality, conformance, and performance of the systems

**Key Projects:**

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| **Project** | Post Silicon validation for MPOS + SF3 SoC |
| **Duration** | Dec 2014 – Mar 2016 |
| **Technology used** | FreeRTOS, arm-gcc, Agilent digital oscilloscope, Ixia, wireshark, YOCTO , Fisheye, PyCharm, Python. |
| **Description** | Characterization of DUTs, SoCs and their individual power consumption in various use-cases and topologies while automating and executing system level tests. MPOS is a point of sale SoC and SF3 is a wired L2 Switch. Automation for test done in object oriented python |

**LSI, Pune  Aug 2009 – Sep 2014**

**Staff System Engineer**

**Accountabilities:**

* Defined software tests in C on emulated and simulated platforms, to eliminate defects in hardware design. Led a team of contractors to accomplish systematic build test and load automation of validation verification test cases.
* Developed verification like tests in C to run on FPGA. Implemented Automated reporting of diagnostic firmware errors/defects using scripting languages like Python and Bash over continuous integration frameworks like Hudson/Jenkings
* Identified & resolved protocol implementation errors & irregularities by testing the phy and its state machines. Deployed error injection and characterized hardware recovery to test for design robustness.
* Developed software to test SATA/SAS phys, spin up controller, enabling signal look up on the logic/protocol analyzer for the purpose of validation.
* Validated tasks on development vehicles like fpga and simulation. Conducted white box / black box testing across various product lines.
* Forward ported validation software from Palladium/FPGA for impending post silicon test phases
* Developed traffic generation/error injection scripts for SAS/SATA devices and characterized the performance and the protocol compliance of the system.

**Key Projects:**

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| **Project** | Validation for Flash Storage Processor |
| **Duration** | Sep 2012 – Sep 2014 |
| **Technology used** | GCC/Gdb, python, SAS/SATA Protocol analyzer, Logic analyzer, Altera phy, Tensilica FPGA, Xtensa OCD, Python, Bash, Hudson/Jenkins, JDSU, DriveMaster |
| **Description** | Validation/verification of hardware design of a flash storage processor (SoC) to develop diagnostic firmware encompassing hardware & testing similarity between emulated / simulated platforms and final silicon |

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| **Project** | SAS/SATA protocol validation |
| **Duration** | Jan 2010 – Aug 2012 |
| **Technology used** | GCC/Gdb, python, SAS/SATA Protocol analyzer, Logic analyzer, Linux Kernel, Multi |
| **Description** | Validation/conformance of a couple of generations of LSI’s HBA (SoC) and expander (SoC) products |

**XStreamHD India, Noida  Jul 2008 – Aug 2009**

**Sr. Systems Engineer**

**Accountabilities:**

* Defined device drivers for SHA, Expt, AES and RTC. Validated DMA hardware encompassing all hardware encryption blocks and DMA to render simplified programming interface (API) for the same
* Developed device driver / validation test routines for Low Noise Block & DiSEqC subsystems of the media receiver. Re-engineered memory management. Implemented mbx graphics accelerator driver

**Key Projects:**

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| **Project** | Media Receiver Board Validation |
| **Duration** | Jan 2009 – Aug 2009 |
| **Technology used** | Metaware IDE/Debugger, ASHLING Opella ICE, ARC C/Assembly |
| **Description** | Hardware encryption block validation |

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| **Project** | Media Server Board Validation |
| **Duration** | Jul 2008 – Aug 2009 |
| **Technology used** | Metaware IDE/Debugger, ASHLING Opella ICE, ARC C/Assembly |
| **Description** | DiSEqC Protocol Driver: DiSEqC is a communication bus protocol between satellite receivers and peripheral equipment. In the Media Server board the DiSEqC hardware connects to a Low Noise Block. MBX Graphics accelerator: MBX is a Open GL compliant graphics accelerator hardware |

**SiRF Technology India Pvt. Ltd.  Nov 2004 – Jul 2008**

**Sr. Systems Engineer**

**Accountabilities:**

* Coordinated activities related to design/implementation of generic I/O driver as well as uart driver. Set up serial nor flash driver and core logic of the code loader, thereby implementing a multi stage boot loader
* Focused on automating test cases for unit and integration testing. Managed changes to firmware to align with hardware/feature enhancements
* Guided team members in bug fixing, route data collection, data plotting and regression testing, implementing NMEA based messages for customization and configuration of receiver driven by customer input
* Set up stack checker, bug tracker (field testing) as well as SDK interfaces using NMEA protocol. Configured power save modes and other configurable GPS parameters like DOP in SSB protocol
* Changed startup code in ARM 7 assembly – for interrupt service in to enable merging of GPS and Bluetooth interrupts. Followed through by merging interrupt handling mechanisms for BT and GPS in C. Implemented POR configuration data read.
* Enhanced efficiency of BT & GPS cores by modifying definitions of 150+ critical applications.
* Built software 16550 based UART device driver, optimizing FIFO usage to create functional specifications for ASIC/FPGA development of an IP Core implementing GPS & Bluetooth capability
* Managed system testing and defect identification across various project phases for ensuring seamless implementation of assigned project

**Key Projects:**

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| **Project** | EZRIP Boot Loader |
| **Duration** | Oct 2007 – Mar 2008 |
| **Technology used** | RVDS 3.0, CodeWarrior ARM C/Assembly |
| **Description** | EZRIP boot loader is written for the next generation of sirf chipsets and reference designs to support loading of firmware from any Serial Flash device supporting the industry standard read command. It also supports code loading from various host port drivers such as uart, I2C and SPI. The boot loader is flexible to load code from either an abstracted host port or from serial nor flash into in place execution capable RAM |

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| **Project** | SiRFDASH DR |
| **Duration** | Jan 2007 – Oct 2007 |
| **Technology used** | ADS 1.2, CodeWarrior ARM C/Assembly. Windows PC, MS MapPoint, Google Earth |
| **Description** | SiRFDASH DR is a range of products which supplements satellite Navigation with Dead Reckoning. GPS receivers, in addition with, MEMS sensors track heading and velocity alongside satellite navigation to provide for better track fidelity and smooth navigation |

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| **Project** | Utilities for SiRFLink1 Firmware |
| **Duration** | 2006 |
| **Technology used** | ADS 1.2, CodeWarrior ARM C/Assembly |

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| **Project** | GPS + BT Core Merge |
| **Duration** | 2005 – 2006 |
| **Technology used** | ADS 1.2, CodeWarrior ARM C/Assembly |

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| **Project** | HSUART Driver |
| **Duration** | 2004 – 2005 |
| **Role** | Sr. Embedded System Engineer |
| **Technology used** | ADS 1.2, CodeWarrior ARM C/Assembly |

Earlier Assignments

**Hexaware Technologies Ltd  Assistant Project Manager  Nov 2001 – Oct 2004**

**Global InfoTech Corporation  Software Engineer  Aug 2000 – Nov 2001**

**HCL Technologies Ltd  Member Technical Staff  Jun 1999 – Aug 2000**

**NexStor India Ltd  Member Technical Staff  Oct 1997 – Jun 1999**

Professional Development

* SAS/SATA
* PCIe
* NVME/AHCI
* Project Management
* Precision Time Protocol (PTP)/ Synchronous Ethernet (Sync E) / Time sensitive networks (TSN)
* NFC

Tools & Technologies

* **Languages:** C, C++, ARM asm, ARC asm, ADSP 21535 asm, Python, BASH, PERL,
* **Hardware:** ARC 600, ARM 7.0, Xtensa (Cadence)cores,PPC
* **RTOS/Embedded:** Thread X, SiRF OS,VXWORKS,uClinux2.4.x, Linux 3.14.x OpenRTOS, FreeRTOS Win CE.
* **Tools:** JDSU SAS\_SATA Protocol Analyzer, Lecroy SATA trainer , Lecroy PCIe Summit analyzer, Teledyne lecryo PE Tracer, GNU Tools, Kgdb, Clearcase, Xilinx FPGA programming suite, Agilent Logic Analyzers and Oscilloscopes (DSO), API2C Exercise, Multi ICE, Soft ICE, Hudson/Jenkins, DriveMaster, OAKGate, Terminal servers, IXIA, WireShark

**Date of Birth:** 08th September 1975 **~ Languages Known:** English, Hindi, French and German **~ Nationality:** Indian

**~ References: Available on Request ~**